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REVIEW

Organic Thin Film Transistors: Materials, Processes and Devices

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Abstract−For the past ten years, organic materials have been extensively investigated as an electronic material for thin film transistor (TFT) devices. Organic materials offer strong promise in terms of properties, processing and cost effectiveness and they can be used in flat panel displays, imagers, smart cards, inventory tags and large area electronic applications. In this review, we summarize the current status of the organic thin film transistors including substrate materials, electrodes, semiconducting and dielectric layers; organic thin film preparation methods; morphological studies for organic thin films; electrical characterization of gate dielectric layers and semiconducting active layers; and characterization of the OTFTs. Future prospects and investigations required to improve the OTFT performance are also given.

Key words: Organic Semiconductors, Organic Thin Film Transistors, Electrical Characteristics, Mobility and Dielectric Property

OVERVIEW OF OTFTS

Transistors based on organic semiconductors (conjugated polymers or small molecules) as active layer to control electric current flow are known as organic thin film transistors (OTFTs). Conduction properties of conjugated polymers or small molecules [Karl, 2002; Lee et al., 2002; Minakata et al., 1992; Brooks et al., 2001; Schön et al., 1998, 2001a, b; Arlauskas et al., 2000; Juska et al., 2000], dielectric properties of insulating polymers [Sakai and Chiang, 2002; Khatipov, 2001; Abd-El-Messieh et al., 2002; Faria and Moreira, 1999; Aihara et al., 1998; Calberg et al., 1999; Araki and Masuda, 2002; Jager et al., 2002; Bistac and Schultz, 1997] and the interface between them are being investigated so that they can be used in OTFTs [Casu et al., 2003; Kymissis et al., 2001; Knipp et al., 2002; Katz and Bao, 2000; Dimitrakopoulos and Malenfant, 2002; Dimitrakopoulos et al., 1996, 1999; Sirringhaus et al., 1999; Schoonveld et al., 2000; Garnier, 1998; Bao et al., 1996; Afzali et al., 2002; Lin et al., 1997; Gundlach et al., 1999; Klauk et al., 1999, 2000a, b; Sheraw et al., 2000; Nelson et al., 1998; Schön et al., 2000; Swiggers et al., 2001; Schön and Batlogg, 1999; Gundlach et al., 1997; Tsumura et al., 1986; Katz, 1997]. OTFTs have the advantage of light weight bendable features along with cost effectiveness and low temperature processing. OTFTs fabricated at low temperatures allow the use of flexible plastic substrates and spin coating process for fast and inexpensive coverage of large areas. Table 1 shows the comparison of inorganic and organic based electronic devices. Single crystal silicon based transistors (MOSFET: metal-oxide-semiconductor field effect transistor) have higher field effect carrier mobility (600-250 cm^2/Vs for electron) than the organic based transistors. Low mobility leads to low frequency operation and this means that organic based electronics will be slower than silicon based circuits. These devices are not expected to compete with silicon technology in the production of high-end products, but they can be components of low speed and low resolution mass produced items. OTFTs will find use in a number of low-cost, large area electronic applications such as liquid crystal flat panel displays, active matrix all organic emissive flat panel displays, imagers, smart cards, smart price and inventory tags, large-area sensor arrays, complementary thin film integrated circuits [Klauk et al., 2000b] and pixel drivers for displays [Katz and Bao, 2000].

Field effect transistors consist of three electrodes--source (S), drain (D) and gate (G)--as shown in Fig. 1. Source and drain are separated by the semiconductor of opposite type (n or p type), whereas the gate is separated from the semiconductor with an insulator. The MOSFET (Fig. 1a), which is a device based on single crystal silicon to control a current between two contacts (source and drain) using a voltage contact (gate), is widely used in integrated circuits. The device uses a surface effect to create an n-type region in a p-type substrate (or the reverse). A negative gate voltage applied to a p-channel field effect transistor forms a channel of positive current (holes) flow and a positive gate voltage applied to an n-channel field effect transistor forms a channel of negative current (electrons) flow. To understand this, we take a simple capacitor structure using a p-type substrate, an oxide layer and a metal gate as shown in Fig. 1a. If we apply a positive potential to the gate (the substrate is grounded), electrons will be attracted to the gate and will pile up at the silicon interface underneath the gate oxide. The basic operation of the device is to bias the gate with $V_G > V_T$ (gate voltage greater than some threshold voltage which is called inversion mode) and form an n-type region between the source and the drain. This provides a simple n-type path between the n-type source and drain regions for electrons to flow. This region is called a channel. Without forming the channel, there are two back to back diodes which will not allow appreciable current to flow between source and drain. The operation mechanism of OTFTs is similar to MOSFET based on single crystal sil-

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‡This paper is dedicated to Professor Hyun-Ku Rhee on the occasion of his retirement from Seoul National University.

Table 1. Comparison of organic and inorganic devices

	Inorganic semiconductor	Organic semiconductor
Field effect carrier mobility	High single crystal silicon: 250-600 cm^2/Vs poly silicon : 40-70 cm^2/Vs a-Si : H: about 1 cm^2/Vs	Low pentacene: 3.2 cm^2/Vs* poly(2,5 thienylenevinylene): 0.22 cm^2/Vs
Toughness	Brittle	Tough
Flexibility	Fragile	Flexible

*: highest reported value [Schön et al., 2000].

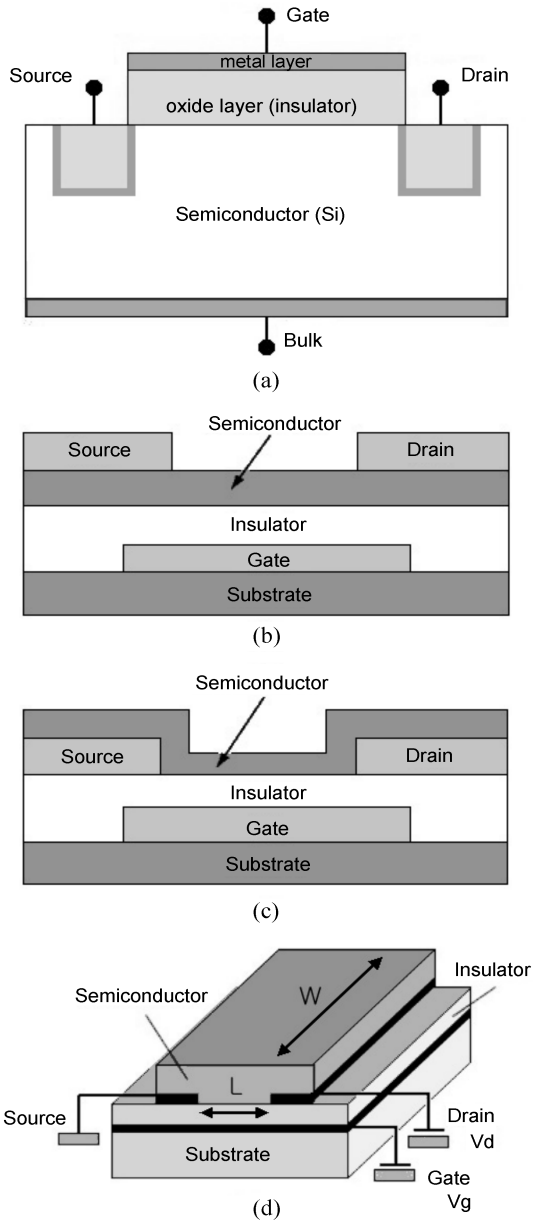


Fig. 1. Device configurations: (a) The schematic of MOSFET. (b) Top-contact device of OTFT, with source and drain electrodes evaporated onto the organic semiconducting layer. (c) Bottom-contact device of OTFT, with the organic semiconductor deposited onto prefabricated source and drain electrodes. (d) 3-Dimensional configuration of bottom contact device of OTFT.

icon. OTFTs can be fabricated as metal-insulator-semiconductor (MIS) type structure as shown in Fig. 1. MIS structure of OTFTs can be fabricated as top contact transistor (Fig. 1b) and bottom contact transistor (Fig. 1c). In the top contact transistor, source and drain regions are deposited above the active semiconducting layer. In the bottom contact transistor, an active semiconducting layer is deposited above the source and drain regions. It is known that the performance of bottom contact configuration is inferior to that of top contact configuration [Kymissis et al., 2001; Schön et al., 2000a; Dimitrakopoulos and Mascaro, 2001]. Basically, the gate turns the semiconductor on and off with applied voltage, thus controlling the source-drain current flow. In the absence of a gate voltage, this device is in an "off" state and no conductivity is observed between source and drain. In MOSFET, doped single crystal silicon in inversion mode is used as an active layer to control the current but TFTs (amorphous silicon, poly silicon or organic TFTs) operate in the accumulation mode in the intrinsic (undoped) semiconductor layer. Upon application of a gate voltage, the channel of charge is formed by attracting opposite charges facilitating flow of current between the source and the drain. In this geometry, there is no depletion layer to isolate the conducting channel from the substrate, and very low conductivity of semiconductor layer is therefore required [Horowitz et al., 1998]. A 3-D configuration of OTFT is shown in Fig. 1d, and performance of the OTFTs can be improved by varying the dimensions and spacing of the source and drain electrodes (which is called gate length, L). Electrical characteristics are strongly influenced by the gate dimensions such as gate width W, gate length L and the gate insulator layer thickness is also crucial to the performance of the OTFTs.

The observed mobilities of organic and hybrid semiconductors are less than that of single crystal or poly crystal silicon. But it is

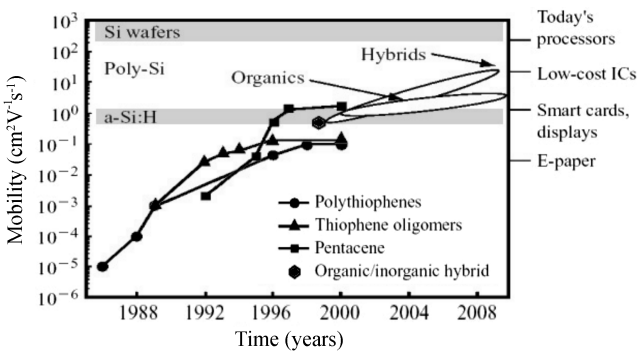


Fig. 2. Performance of organic and hybrid semiconductors.

almost in the range of mobility observed for hydrogenated amorphous silicon (a-Si:H), which is now used as a thin film transistor (TFT) in liquid crystal display applications. Hybrid semiconductors will have mobility higher than a-Si:H in the near future and will find applications in low cost integrated circuits. Conjugated organic materials have the ability to conduct charge (holes and electrons) due to the π-orbital overlap of neighboring molecules. Carrier mobility has been improved either by selecting compounds with better characteristics or by considering hybrids of organic and inorganic materials. Fig. 2 shows the performance of organic and hybrid semiconductors compared with inorganic semiconductors [Denis Sweatman, 2001].

Highly conjugated organic materials have the potential to work as semiconductors because of their strong π-orbital overlap. In organic solids, the carbon atom forms a tetrahedral SP^3 hybridized single bond configuration, but in double bond it has the configuration of SP^2-P_z and in triple bond it has SP-P_z-P_y configuration. The intra-molecular interactions between the atoms lead to a splitting of the initially degenerated $2P_z$ energy levels into a bonding and an anti-bonding molecular π orbital. The resulting bonding orbital takes the electrons while the anti-bonding orbital remains empty. On a downward positive electron binding energy scale, there is the highest occupied molecular orbital (HOMO) and a lowest unoccupied molecular orbital (LUMO) with an energy gap in between. For larger conjugated carbon-carbon double bond systems further splitting occurs. Also, intermolecular interactions in the solid lead to the further splitting of these molecular levels under formation of narrow bands and the energy gap decreases as well. Depending on the nature of the semiconductor and electrode used, the channel formed can be n-channel, where electrons are the charge carriers, or p-channel where holes are the charge carriers. When an electron is added or a hole is injected, the resultant charge becomes delocalized across the conjugated system. This injected charge is able to act as a carrier for current through the molecule. An effective organic semiconductor must have a redox potential that is open to charge injection by a small applied voltage. In other words, the HOMO for hole injection or the LUMO for electron injection must be energetically accessible. On the other hand, the orbitals should not be so easily accessible that the semiconductor can be effectively turned off (have a high I_{on}/I_{off} ratio). The parameter that is more likely to become a deciding factor for FET application is an organic materials capacity to form a continuous thin film that, when turned on, allows charge to move through at a quick enough pace for use in actual electronic applications. Organic thin films are amorphous or crystalline collections of molecules interacting through weak Van der Waals forces. In this case, the charge carriers move via hopping between localized molecular π orbital (slow process). The energy gap between HOMO and LUMO is normally 1 to 4 eV, so that electrons can jump with small effort to the LUMO level and contribute to conduction. Charge transport is then relatively easy within a molecule, but due to the disordered molecular structure of the most organic semiconductors, charge transport between molecules is much more difficult. A model that is often used to describe organic semiconductors explains transport between molecules (or more generally between localized states) as a thermally activated charge carrier tunneling (hopping). Hopping occurs between localized states that are disordered both in space and energy [Cantatore, 2000].

With the intermolecular structure more ordered, the hopping between molecules will be easier. This means that mobility will be better in semiconductors that have a well-organized molecular structure. Organic semiconductors have poor self-organizing properties, due to their weak London or Van der Waals intermolecular bonds. To improve the structural organization of organic thin film, Garnier et al. suggested raising the deposition temperature of the organic layer. Experimental results showed that the morphology of the sexithiophene (6T: Fig. 4) film had the appearance of polycrystalline of increasing grain size when substrate temperature was raised [Garnier, 1998]. Recent measurements of pentacene TFTs at various temperatures showed that mobility was increased when the measuring

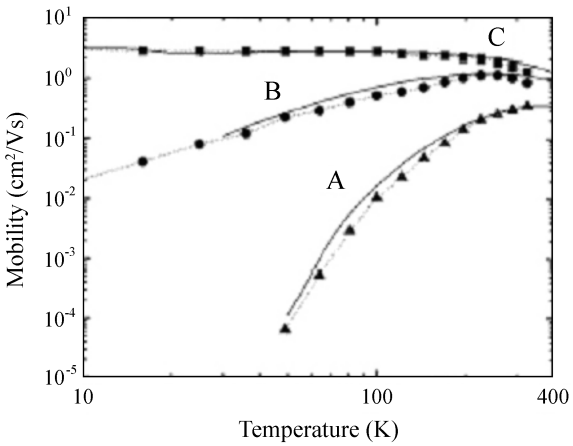
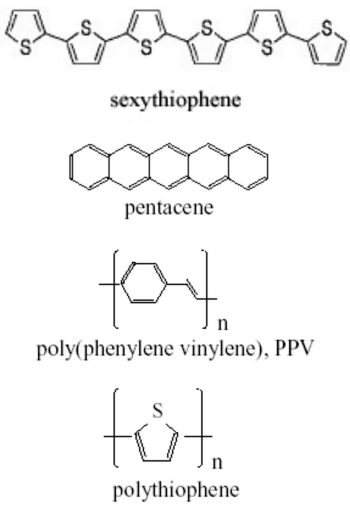


Fig. 3. Field-effect mobility vs. temperature for pentacene thin film devices [Schön and Batlogg, 1999]. Samples A, B, and C were made under similar conditions.



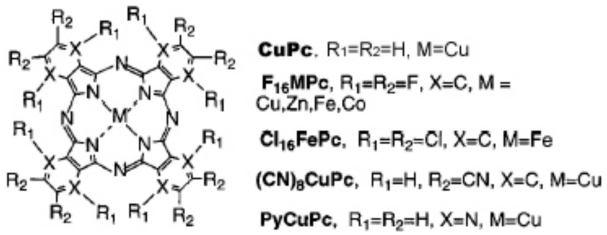


Fig. 4. Molecular structures of typical organic semiconductors.

temperature was increased. Fig. 3 shows the field effect mobility of pentacene in various temperatures. At very low temperature range, the Fermi level is close to the band edge and the trap levels are unoccupied and neutral. Hence, the band bending at the grain boundaries vanishes and the mobility is high. With increasing temperature, the Fermi energy moves towards the middle of the gap and electrons fill trap states. Then the grain boundary charges up negatively and a potential well forms. In this case, charge carriers fall into the well, lose their energy by scattering and are thermally re-emitted. A further increase in temperature leads to a higher probability for the charge carriers to escape from the well, which leads to an increased mobility [Schön and Batlogg, 1999].

MATERIALS FOR SUBSTRATE, ELECTRODE, SEMICONDUCTING LAYER AND DIELECTRIC LAYER

1. Substrates

Materials such as quartz, polycarbonate, polyethylene naphthalate (PEN), polyimide, polyethylene, glass, silicon wafer can be used as a substrate to form OTFTs [Dimitrakopoulos et al., 1999; Garnier, 1998; Klauk et al., 2000a, b, 2003; Li et al., 1998]. Inorganic substrates such as quartz, glass, and silicon wafer have high melting point, good flatness and low diffusivity of chemicals and air. On the other hand, polymer substrates such as PEN, polyethylene terephthalate (PET), and polyimide have high toughness, flexibility and light weight. In particular, PEN, PET, and polyimide have comparatively high toughness and thermal resistance, so these polymers are feasible for substrate materials of organic electronic devices. Silicon wafer can be used as a substrate as well as a gate electrode. It is important to clean the substrates to remove contaminants and impurities present on the substrate surface before depositing the film. Surface preparation of silicon wafers is done either by degreasing with organic solvents and cleaning with inorganic acids [Bhat et al., 1999]. Glass substrates are cleaned by rinsing in a solution of detergent and deionized water in an ultrasonic bath followed by boiling in 1,1,1-trichloroethane, rinsing in acetone, and rinsing in 2-propanol [Baldo et al., 1997]. Flexible substrates are rinsed with detergent and 2-propanol solution.

2. Electrodes

Metals such as gold, platinum, aluminum, magnesium, palladium, chromium prepared by evaporation [Schön et al., 2000; Xu et al., 2000; Li et al., 1998], poly-3,4-ethylenedioxythiophene (PEDOT) and graphite based inks prepared by inkjet printing, and polyaniline doped with camphorsulphonic acid (PANI-CSA) deposited by spin coating [Garnier, 1998; Cantatore, 2000; Okubo, 2001] have been used as electrodes in many experiments. Adding nickel on gold improves adhesion of the gold on the oxide. Gold electrodes work slightly better than platinum electrodes. Palladium (relatively large work function) is expected to improve carrier injection into the organic semiconductor. Low work function metals such as magnesium (Mg) or aluminum (Al) gave slightly higher electron mobility (2.2 cm^2/Vs at room temperature, up to 3×10^4 cm^2/Vs at low temperatures) in single crystals [Schön et al., 2000]. In order to improve the transport in thin film devices, a detailed understanding of the trapping process and the charge injection is required. Work functions of source and drain contacts strongly influence the I-V relationships of OTFTs. The work function of Au is 4.7 eV and HOMO of most of the organic semiconducting materials are around this level, so between Au and organic semiconductor, ohmic contact can be formed and electrical characteristics can be improved. On-current of OTFTs can be increased by shrinking the effective channel length (L). Top contacts seem to work far better than bottom contacts. Bottom contacts are worse because grain boundaries that form at the edge of the electrodes extend into the channel. Top contacts must be formed with shadow masks and bottom contacts can be formed photo-lithographically.

3. Semiconducting Layer

Fig. 4 shows some of typical organic semiconducting materials. The most successful and widely studied organic semiconductor molecules are pentacene [Schön et al., 2001b; Garnier, 1998; Afzali et al., 2002; Nelson et al., 1998; Klauk et al., 2000b; Gundlach et al., 1997; Katz, 1997; Necliudov et al., 2003; Horowitz, 1998] and thiophenes [Dimitrakopoulos et al., 1999; Lovinger and Rothberg, 1996; Crone et al., 2000; Peng et al., 1990; Bolognesi et al., 2003; Sirringhaus et al., 1998, 1999]. Though small-molecule organic semiconductors have higher mobility than polymer semiconductors like PPV or polythiophene, most of those have lower solubility in the organic solvents. The mobility of phthalocyanine (Pc) is relatively high (0.02 cm^2/Vs) for a p-channel OTFT based on CuPc (Fig. 4) [Bao et al., 1996]. A dramatic change in the OTFT characteristics was observed with metallophthalocyanine derivatives (Fig. 4: F_{16}MPc, Cl_{16}FePc, $(CN)_6$CuPc, PyCuPc) bearing electron withdrawing groups. The OTFTs behaved like n-channel semiconductors instead of p-channel semiconductors [Bao et al., 1998]. This opposite of the channel activity is a result of the charge in the LUMO energy level of the molecule caused by the electron-withdrawing groups, making the orbital more accessible for electron injection. The best mobility, around 0.02 cm^2/Vs was exhibited by the fluorinated derivative (Fig. 4: F_{16}CuPc) at 125 °C of deposition temperature and on/off ratio of 5×10^4 was observed.

Table 2 shows the mobility and on/off current ratio measured from OTFT by using organic molecules deposited by different techniques. The highest value of pentacene is similar to that of a-Si:H. Recently, the acene groups as an active layer in OTFTs have been studied extensively because of their electrical properties. While lower [n] acenes (n=2-3) are insulators, higher [n] acenes (n=4-5) show semiconducting behavior. Poly[n]acenes are calculated to be conductors and predicted to be superconductors [Herwig and Müllen, 1999; Schön, 2001]. Table 3 shows the value of mobility reported by Schon et al. [2001], for acene films deposited by vapor phase deposition. Though tetracene shows very impressive mobility, no field effect was observed in tetracene according to Herwig and Müllen [1999]. Among all investigated oligomeric and polymeric materials, pentacene thin films have demonstrated the best electrical performance. Pentacene exhibits typical p-channel semiconductor characteristics. Field effect mobility exceeding 3.2 cm^2/Vs, on/off ratios of $>10^8$, sub-threshold swings below 1 V/decade and near zero threshold at room temperature has been reported [Schön et al., 2000a; Schon, 2001]. At low temperatures (below 250 °K), very high mobility values from 400 cm^2/Vs to more than 1,000 cm^2/Vs have been reported [Schön et al., 2000; Dimitrakopoulos and Mascaro, 2001; Karl et al., 1991]. The high mobility of pentacene is a result of significant orbital overlap from edge-to-face interactions among the molecules in their crys-

Table 2. Mobility (μ) and on/off current ratio of OTFTs

Material	Mobility cm^2/Vs	I_{on}/I_{off}	W/L	Dep. method	Ref.
Copper phthalocyanine	0.01-0.02	NR	NR	V*	29
Pentacene	2.7	10^9	20-70	V	36
Polythiophene	~10^{-5}	>10^2	NR	S**	42
Pentacene	1.5	10^8	2.5	V	49
Pentacene	3.2	10^9	250-1,000	V	52
Pentacene	0.21	>10^6	1,000	S	63
Pentacene	0.9	10^6	1-20	S	64
P3HT	0.1	>10^6	NR	S	65
Poly-3-hexylthiophene (P3HT)	0.96×10^{-4}	NR	NR	S	66
Diphthalocyanine	10^{-3}	NR	12	V	67
Polyacetylene	4×10^{-5}	NR	180	S	68
Alpha-sexithienyl	3.3×10^{-4}	NR	3.44	V	69
Poly(2,5 thienylenevinylene)	0.22	NR	1,000	S	70
C_{60}	0.3	NR	400	V	71
α-ω-hexathiophene	0.03	>10^6	21	V	72
Poly(3-hexylthiophene)	0.015-0.045	4×10^5-10^4	20.8	S	73
Pentacene	10^{-4} -10^{-2}	~10^5	>150	S	74
Bis(dithienolthiophene)	0.05	10^8	500	V	75
Pentacene	0.7	10^7	11	V	76
BTET	0.001	NR	~17	S	77
α-ω-dihexyl-hexathiophene	0.13	>10^4	7.3	V	78
Poly-3-hexylthiophene	0.1	10^6	NR	S	79
DHα4T	0.039	NR	4	V	80
α,ω-Dialkyl thiophene	0.01	>10^4	NR	S	81
PAPSAH	2.14	36.64	NR	S	82
ADT	0.15	NR	1.5-4	V	83
Pentacene	0.15	NR	NR	V	84
Pentacene	0.38	NR	4	V	85

*: Vapor based deposition method.
**: Solution based deposition method.

Table 3. Mobility of acene groups

Material	$\mu_{RT,p}$ (cm^2/Vs)	$\mu_{max,p}$ (cm^2/Vs)	$\mu_{RT,n}$ (cm^2/Vs)	$\mu_{max,n}$ (cm^2/Vs)
Anthracene	2.3	2×10^8	1.6	500
Tetracene	2.7	2.5×10^5	1.8	3×10^4
Pentacene	3.2	10^5	2.3	2×10^4

tal lattice. These kinds of interactions are characteristic of herringbone geometry as illustrated in Fig. 8c. This geometry maximizes π-orbital overlap [de Wijis et al., 2003].

Pentacene thin films deposited by dry process at very low pressures (evaporation) showed better crystallinity and mobility than films deposited by wet process like spin coating with a solution. Spin coating is relatively simple and cost effective but the solubility of pentacene in most solvents is quite low. To overcome the low solubility in organic solvents, researchers have prepared functionalized pentacene derivatives (or pentacene precursor which leads to pentacene upon annealing) with better solubility. In the solution processing method, continuous, amorphous thin films of pentacene can be obtained when pentacene precursor dissolved in suitable solvents is spun onto substrates with subsequent evaporation of the

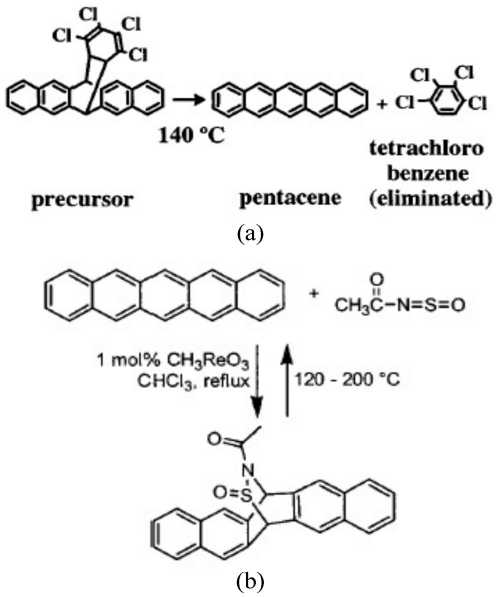


Fig. 5. Chemical schemes for the conversion of the precursor into pentacene: (a) pentacene precursor by the method of Herwig et al. (b) pentacene precursor by the method of Ali Afzali et al.

solvents [Afzali et al., 2002; Brown et al., 1997; Dodabalapur et al., 1995]. Fig. 5 shows chemical reactions for the conversion of the precursor into pentacene. The conversion to pentacene crystal is accomplished by heating the films at a temperature of 140-220 °C in vacuum from several minutes to 2 hours [Herwig and Müllen, 1999] by Herwig et al. (Fig. 5a). Recently, IBM developed a pentacene precursor which dissolves in chlorinated hydrocarbons, THF and dioxane and may be stored for months at −10 °C without decomposition (Fig. 5b). Precursor route has the advantage of solution processing with converted films only of a conjugated backbone. The absence of solubilizing side groups may increase the π-π overlap, which again improves the charge transport.

Pentacene can be thermally evaporated in vacuum at a pressure above 10^{-5} Pa on a substrate kept at 60 °C [Dimitrakopoulos and Malenfant, 2002; Klauk et al., 2000b]. Monocrystalline films show the highest mobility of 2.7 to 3.2 cm^2/Vs [Schön et al., 2000a, b; Cantatore, 2000]. Molecular beam deposition in vacuum shows the mobility of 3.8×10^{-2} to 0.038 cm^2/Vs [Cantatore, 2000; Brown et al., 1996] and solution processed films from precursor shows mobility of 10^{-2} to 0.2 cm^2/Vs [Cantatore, 2000; Herwig and Müllen, 1999].

Since the active layer is grown on gate insulators, the surface chemical state of the insulator has an impact on the morphology of the active layer grown on it. Larger pentacene grains can be obtained with chemical processing of the gate insulator before pentacene deposition. Monolayer of organic cyclohexane coated over gate dielectric gave pentacene crystal grains of 0.5 to 2.5 micron in size. This is 20 to 100 times larger than that grown without surface processing [Okubo, 2001].

4. Dielectric Layer

The dielectric material needs to have very high resistivity to prevent the leakage between gate metal and semiconductor channel and highest possible dielectric constant to have enough capacitance for channel current flow. High dielectric constant insulators result in low switching voltage of the OTFTs. Table 4 shows the important dielectric materials that can be used for OTFTs. OTFTs with high dielectric constant inorganic insulators such as tantalum oxide (Ta_2O_5) or barium zirconate titanate (BZT) showed low voltage operating characteristics [Dimitrakopoulos et al., 1999; Bartic et al., 2002]. Dielectric films are deposited by chemical or physical vapor deposition for inorganic materials and spin coating for organic materials. Fig. 6 shows the molecular structure of PMMA and cyanoethylpullulan (a kind of cyano resin). Polymethyl methacrylate (PMMA)

Table 4. Dielectric materials for OTFTs

Dielectric material	Dielectric constant	Preparation method	Properties
Benzocyclobutane (Cyclotene™)	2.65	Spin coating	Low moisture uptake
PMMA#	2.5-4.5	Spin coating	Unaffected by moisture
Octadecyltrichlorosilane	-	Spin coating	-
Polyimide (BMT, ZTS)*	2.6-3.3	Spin coating	-
Teflon AF^R (AF1600 or AF2400)*	1.9	Spin coating	-
Spin on glass (SOG)	3.9-5	Spin coating	-
Fluorinated benzoxale copolymer	2.2-2.3	Spin coating	Low water absorption
OCD T7	~3	Spin coating	
OCD T2	~3	Spin coating	
HSG##	~3	Spin coating	Low water absorption
Flare (Fluorinated Poly(ArylEther)	~2.5	Spin coating	Low water absorption
DVS-BCB (siloxane Bibenzocyclobutene)	~2.5	Spin coating	Low water absorption
Poly(tetrafluoro-p-xylylene)	~2.42	CVD	Stable
AF-4###	~2.28	CVD	Stable
Polysilsesquioxanes	2.6-2.9	Spin coating	-
AlN	9-10.4	Sputtering	-
Barium zirconate titanate (BZT)	17.3	Sputtering	-
BZT	27-30	Thermal oxidation	Process temp. is high
BZT	3.1	Vapor deposition	Process temp. is RT
$PbZrTiO_3$(PZT)	-	Sputtering	-
PVDF +$BaTiO_3$	40	Spin coating	-
PVDF####	12	Spin coating	-
Cyano resin	18	Spin coating	-
P(VDF-TrFE) copolymer	>40	Spin coating	-
Al_2O_3	9	Sputtering	-
Ta_2O_3	26	Sputtering	-

#: polymethylmethacrylate
##: tantalium oxide
###: parylene
####: polyvinylidene fluoride

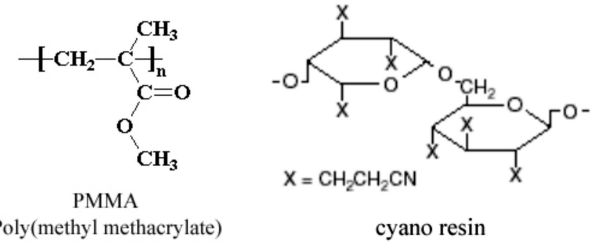


Fig. 6. Molecular structures of feasible organic dielectrics.

is known to adhere well to pentacene and boost carrier mobility. Compared to SiO_2 gate insulator, carrier mobility is increased about 10 times to 0.28 cm^2/Vs [Okubo, 2001]. Cyano resins are reported as high dielectric constant organic material [Sakai and Chiang, 2002]. The dielectric and active layer interface is very important for the transistor characteristics and smooth interface with minimum amount of defects are required.

5. Thin Film Characterization

It is desirable to characterize the organic semiconductors (used as active layer), dielectric insulator materials and the interface between these two layers. XRD, AFM and SEM are used for structural analysis of organic semiconductor layer and dielectric insulator layer. Scanning probe techniques such as atomic force microscopy (AFM) and scanning electron microscopy (SEM) are found to be very useful to study the structure of the organic films coated over the substrate. Fig. 7 shows an example on the relationship of the morphology and process conditions measured by SEM. Processing variables (pressure, substrate temperature, substrate morphology, surface tension, etc.) are known to influence the morphology of pentacene. The higher the temperature of the substrate, the bigger the crystal size that is grown on it. Also the device with octadecyltrichlorosilane (OTS) treated dielectric shows higher field effect mobility [Stein et al., 2002]. Self assembled monolayer of OTS is made by Langmuir-Blodgett (LB) method. Crystallinity is increased and the defects among pentacene grain boundaries are reduced because OTS treated substrate becomes hydrophobic. Self-organizing materials such as OTS are attractive because they allow the formation of an ordered template as shown in Fig. 8 [Kymissis et al., 2001] on an amorphous substrate such as SiO_2 or perhaps a polymer. SiO_2 surface has lower surface energy than OTS coated surface. Normally, higher attraction is expected to lead to smoother and more highly ordered patterns. This is not the case with pentacene since repulsion from the substrate is essential for favorably ordered growth. Growth of the large-grained first layer of pentacene is not observed on metals because the effective surface energy of metal is low. Absence of repulsion between the pentacene backbone and the substrate causes a fraction of the admolecules to lie flat on the substrate during condensation which prevents lateral ordering, and a different nonplanar form of the material occurs on the metal contacts [Kymissis et al., 2001]. So it is expected that the structure of pentacene is easy to be like Fig. 8b on the lower effective surface energy substrate. Structural properties such as amorphous or crystalline nature, evolution of the surface structure, adsorption of molecules, interfacial interactions, dislocations, aging and annealing effects can be observed using AFM and SEM [Dimitrakopoulos et al., 1996; Lin et al., 1997a; Gundlach et al., 1997; Dimitrakopoulos and Mascaro, 2001; Xu et al., 2000; Li et al., 1998; Cristescu et al., 2003]. X-ray diffraction (XRD) can be used to measure the crystallinity of the organic films [Dimitrakopoulos et al., 1996, 1999; Lin et al., 1997a, b; Gundlach et al., 1997; Sirringhaus

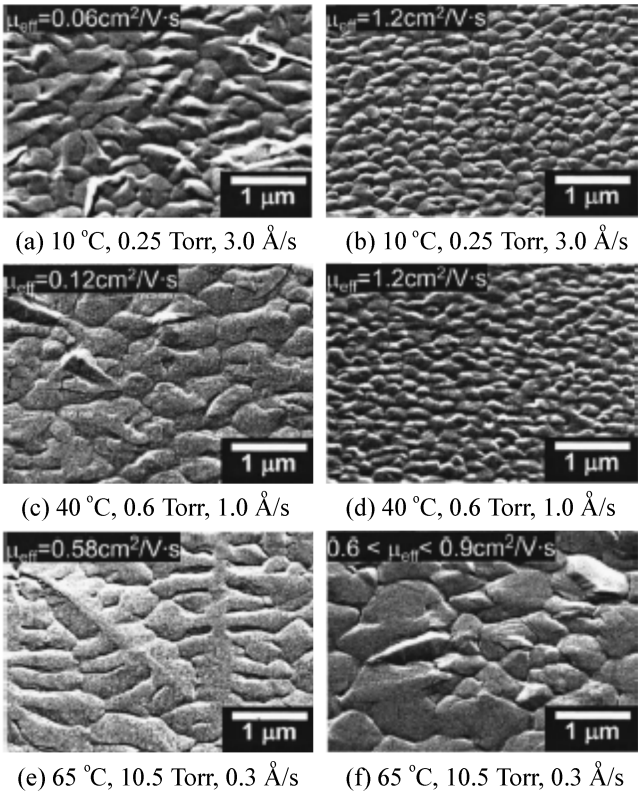


Fig. 7. Scanning electron micrographs of pentacene thin films deposited by organic vapor phase deposition onto SiO_2 (left column) and onto SiO_2 pretreated with octadecyltrichlorosilane (right column).

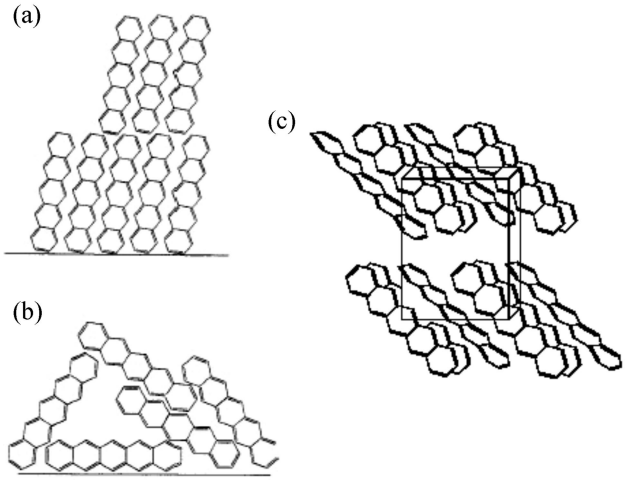


Fig. 8. (a) Schematic diagram of ordered packing state, with substrate repelling pentacene molecules. (b) When the pentacene is attracted to the substrate material, as is the case with metals, the ordered packing state cannot form. (c) The herringbone motif found in pentacene crystalline thin films.

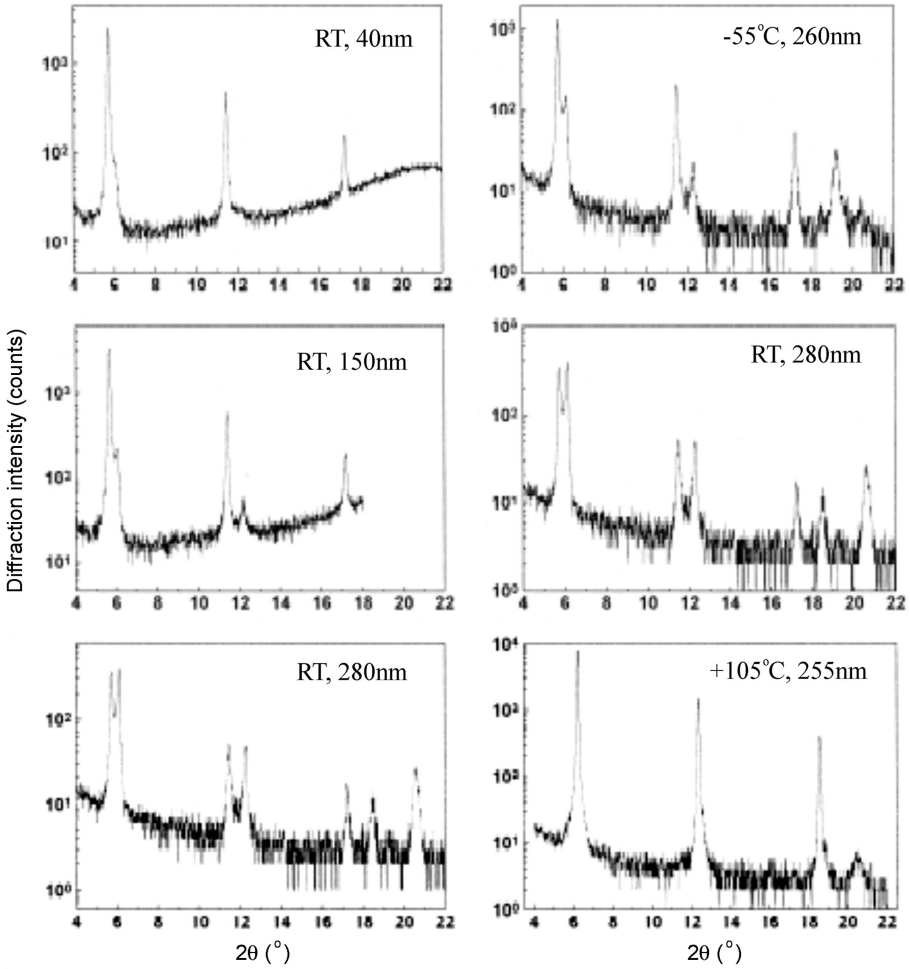


Fig. 9. X-ray diffraction measurements of pentacene films. Left hand side: different average film thicknesses for constant preparation temperatures. Right hand side: different preparation temperatures for nearly constant average film thickness.

et al., 2000; Salih et al., 1998; Xu et al., 2000; Xie et al., 2003; Kim et al., 2002]. Fig. 9 shows X-ray diffraction measurements of pentacene films. The left column shows the XRD peaks of the pentacene layer with different film thickness but grown at the same temperature, and the right shows the peaks of the sample with same thickness but grown at different temperatures. It gives an insight into the molecular organization on a microscopic scale. It shows that the 'metastable thin film phase' is dominant in the film grown at room temperature and with average film thickness smaller than 50 nm. But the 'single crystalline phase' is dominant in the film grown at higher substrate temperatures and with thickness above 150 nm. Single crystalline phase was observed with deposition temperatures higher than 100 °C [Jentzsch et al., 1998]. Polarized microscopy can be used to obtain assembly properties of the polymer or oligomer on a macroscopic scale [Lin et al., 1997a]. UV-Vis electronic absorption spectroscopy can be used to get information about electronic transitions, band gaps, and chromic effects of organic materials [Dirnitrakopoulos et al., 1997; Chen et al., 1995].

ORGANIC THIN FILM PREPARATION

Thin films of organic molecules can be prepared by vacuum deposition [Bao et al., 1996; Schön et al., 2000a, b; Lin et al., 1997b], low pressure vapor phase deposition (LPVPD) [Baldo et al., 1998; Shtein et al., 2001; Burrows et al., 1995], pulsed laser deposition [Li et al., 1998; Cristescu et al., 2003], Langmuir-Blodgett (LB) [Xu et al., 2000, 2003], and solution processing methods such as solution casting, spin coating, spray coating and printing [Dimitrakopoulos and Mascaro, 2001; Klauk et al., 2003; Brown et al., 1997; Chopra and Kaur, 1983; Kim et al., 2002]. So far, vacuum deposition remains the best performer because very well ordered structures can be obtained resulting from the use of highly controllable deposition conditions. It is appropriate for the deposition of molecular materials over small substrates. Solution processing methods such as solution casting, spin coating and printing attract much attention because of their cost effectiveness. Soluble organic polymers and oligomers can be deposited by solution processing techniques. In the solution processing technique, film formation takes place by evaporation of the solvent from a polymer solution. The thickness of films as small as 5-10 nm may be deposited by using dilute and low viscous solution [Chopra and Kaur, 1983]. Compared to spin coating, the mobilities of the films obtained from solution cast are normally higher because slow evaporation of the solvent enables slower growth of the films and therefore allows ordering [Kim et al., 2002]. These

solution processing methods have problems with film thickness and compositional uniformity. Compared to vacuum and spin deposition methods, organic vapor phase deposition (OVPD) has the advantage of using carrier gases to transport source materials to a substrate. The following paragraphs give an insight of the vacuum deposition, OVPD, and spin coating methods.

Vacuum deposition is the deposition or coating of a film in a vacuum environment. Generally, the term is applied to processes that deposit atoms or molecules one at a time from the gas phase, such as in physical vapor deposition (PVD) or low-pressure chemical vapor deposition (LPCVD) processes. Fig. 10a shows a schematic of a vacuum evaporator. The vacuum in the deposition process increases the "mean free path" for collisions of atoms and high-energy ions and helps reduce gaseous contamination to an acceptable level. Vacuum evaporation (including sublimation) is a PVD process where gaseous molecules from a thermal vaporization source reach the substrate surface without collisions in the space between the source and substrate. The base pressure of the deposition system is an important deposition parameter because it determines the mean free path of the sublimed organic semiconductor molecules and the presence of unwanted atoms and molecules in the vicinity of the substrate surface during the film formation. Typically, vacuum evaporation takes place in a gas pressure range of 10^{-5} to 10^{-9} Torr, depending on the level of contamination that can be tolerated in the deposited film. Deposition rate monitoring and control are relatively easy in vacuum deposition compared to the other techniques. Organic semiconductor films can be deposited by sublimation in a variety of vacuum deposition systems [Dimitrakopoulos and Malenfant, 2002; Schön et al., 2000a, b; Lin et al., 1997b]. Thin film morphology and the transport properties of OTFTs are influenced by substrate temperature, deposition rate, purity of the organic source material and substrate cleanliness. Pentacene thin films are

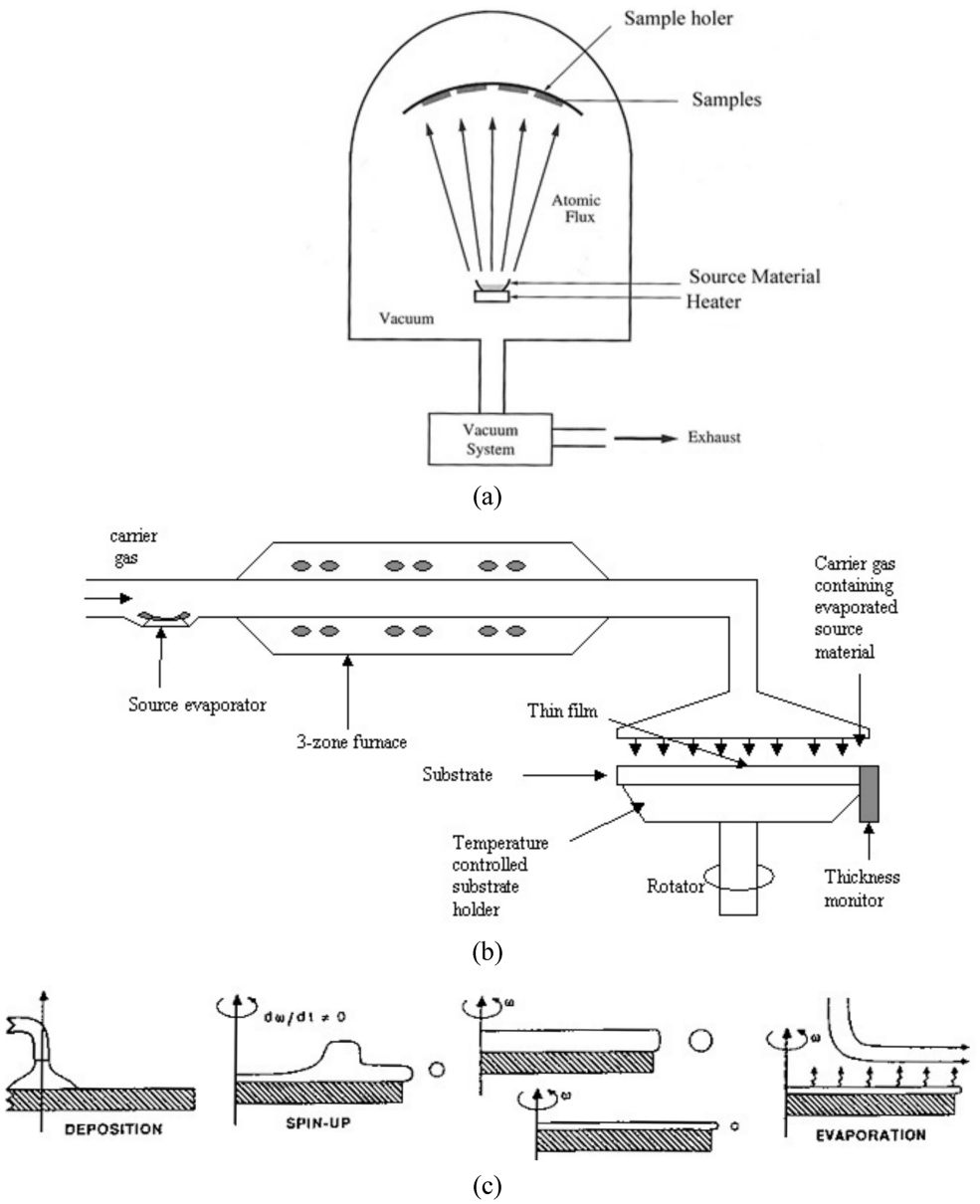


Fig. 10. The schematic of organic thin film processing: (a) vacuum evaporator. (b) organic vapor phase deposition (OVPD). (c) spin coating.

intolerant to exposure to the various chemicals used in a typical lithographic process. So, shadow masking is generally used to pattern the source and drain contacts on top of the pentacene [Xu et al., 2000].

In OVPD, the organic molecules are thermally evaporated into streams of inert gas and transported to a cooled substrate where condensation occurs. It enables low cost fabrication of OTFTs [Baldo et al., 1998; Shtein et al., 2001; Burrows et al., 1995] because the operating pressure is relatively higher than vacuum deposition. The OVPD offers the ability to precisely control the multi-source deposition and uniform deposition of organics on large area substrates. Carrier gas is allowed to flow inside of the barrels to pick up the organic vapors and transport them downstream towards the substrate. The vapor deposition of organic materials is performed below atmospheric pressure (≤10 Torr) to improve the film uniformity. A system of OVPD, more suited for mass fabrication, is shown in Fig. 10b. In this system, the sources are positioned outside of the deposition tube and only the gas flow is used to regulate deposition rate and film thickness. The uniformity of film thickness over the substrate is ensured by a distributor showerhead placed near the substrate.

Spin coating involves the acceleration of a small liquid droplet on a rotating substrate. Fig. 10c shows a schematic of the spin coat process. The coating material (in solution form) is dropped on the center of the substrate either manually or by mechanical arrangement. The spin coating technique consists of the following basic stages: 1) the polymer solution is dispensed onto the substrate, 2) the polymer solution is spread across the substrate (by spinning at approximately 500 rpm), 3) the wafer is then spun at a higher speed (2,000-5,000 rpm), 4) the "thickened edge" is removed by using a backside wash cycle which causes solvent to curl back over the lip of the substrate and wash off the bead that is created due to the surface tension at the edge of the substrate. Spin coating is the preferred method for making thin, uniform films on flat substrates [Dimitrakopoulos et al., 1999; Lovinger and Rothberg, 1996; Crone et al., 2000; Peng et al., 1990; Bolognesi et al., 2003].

DEVICE OPERATION OF OTFT

Electrical properties of each layer including dielectric and semiconducting layer are important and their effect on final transistor performance should be elucidated to get an optimized transistor configuration. In this section, major parameters in transistor performance and their relationship with thin film properties will be summarized, and in the next section, electrical properties of each layer along with characterization method will be described.

1. Field Effect Mobility (μ_{FET})

A common measure used to determine the processing speed of FETs is field effect mobility (μ_{FET}), which is the average charge carrier drift velocity per unit electric field. It is a measure of how easily charge carriers can move in the device. Large field effect mobility is the key to obtaining a large on current for a given device geometry and gate dielectric. The essential prerequisite for TFTs is 1) large field effect mobility, 2) large on/off current ratio (I_{on}/I_{off}), 3) small sub-threshold slope, and 4) near zero threshold voltage. Low sub-threshold slope and near zero threshold voltage reduce the power consumption of an integrated circuit (IC). Silicon transistors have mobility values well over 100 cm^2/Vs, while the best performance organic semiconductors have generally ranged between 0.1 and 3.2 cm^2/Vs [Dimitrakopoulose et al., 1999; Sirringhaus et al., 2000; Schön et al., 2000b]. High mobility is desirable to increase the maximum frequency of operation, f_{max} of OTFT. The maximum frequency can be explained by the response time of the field effect transistor which is defined as the time in which the change in the drain current makes up the change in the total charge on the gate, that is [Grove, 1967],

Table 5. Operating frequency for images

Operating requency	Image
Several Hz	Electronic paper TFTs for displaying still images
1 kHz	TFTs capable of handling moving images
1 MHz	Round displays capable of being rolled up

$$f_{max} = \frac{g_m}{C_G} = \frac{\mu_{FET} V_D}{L^2} \quad (1)$$

where g_m, $C_G = C_i LW$, μ_{FET}, V_D, L are transconductance, the total gate capacitance of the device, field effect mobility, drain voltage and channel length respectively. The minimum value of the field effect mobility needed to drive liquid crystal display pixels is 0.1 cm^2/Vs and for smart card is around 1 cm^2/Vs. Table 5 shows the value of the operating frequency required for handling images. Operating frequencies rise with the field effect mobility of the semiconductor material. The frequency can be raised either by developing organic materials with high field effect mobility or by improving the structure of the transistor. Operating frequency of 1 MHz in display peripheral circuits using organic molecules will require channel lengths under 1 micron.

Higher field effect mobility can be achieved by reducing the number of grain boundaries and the crystal grains per unit area. The size of the crystal grain is strongly dependent on the base material under the deposited film. The base layer in metal-insulator-semiconductor (MIS) structure is gate dielectric film. Grains grow around the core of impurities in the gate dielectric film surface. Grain boundaries are high-volume and low-order regions that contain many morphological defects linked to the creation of charge carrier traps in the band-gap. These morphological defects can be considered responsible for the reduced performance of TFTs [Garnier, 1998; Schön et al., 2000b; Meyer Zu Heringdorf, 2001]. Field effect mobility is a parameter related to the absolute quantity of 'on' current (I_{on}) that can be induced in the device. Mobility can be determined from the plot between drain current (I_D) versus drain voltage (V_D) for various gate voltages (V_G) [Garnier, 1998; Assadi et al., 1988; Xu et al., 2000]. A typical plot of drain current versus drain voltage at various gate voltages is shown in Fig. 11a [Lin et al., 1997a]. I_D increases linearly with V_D at low V_D values and it is determined from the following equation,

$$I_D = \frac{WC_i}{L}\mu_{FET}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \quad (2)$$

where W is the channel width, C_i is the capacitance per unit area of the gate insulator, V_T is the threshold voltage and μ_{FET} is the field effect mobility. μ_{FET} can be calculated in the linear regime from the transconductance (g_m) [Dimitrakopoulos et al., 1997; Garnier et al., 1998; Xu et al., 2000]

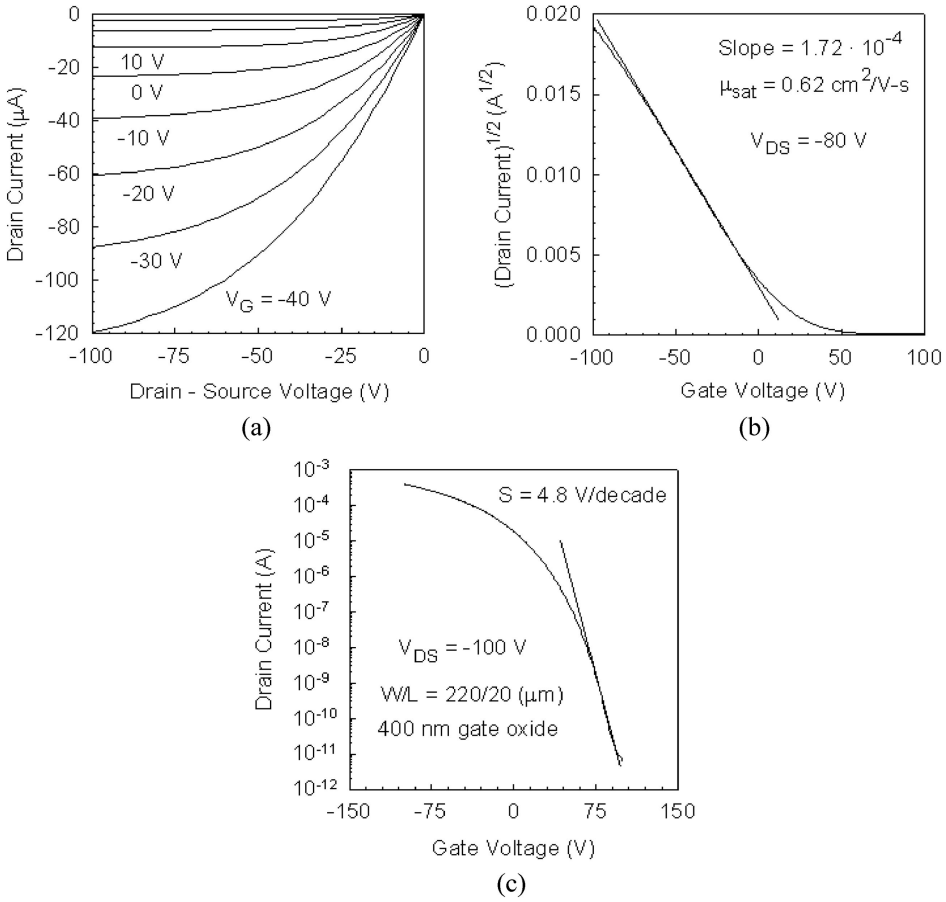


Fig. 11. Typical I-V curve for pentacene TFT: (a) drain current (I_D) vs. drain-source voltage (V_{DS}) characteristics at various gate voltage. (b) I_D vs. gate-source voltage (V_{GS}) characteristics plot to calculate saturated field effect mobility and sub-threshold swing. (c) $Log_{10}(I_D)$ vs. V_{GS} characteristics for the pentacene TFT of Fig. 11b. The TFT on/off current ratio is greater than 10^8 even with V_{DS} biased as −100 V.

$$g_m = \left(\frac{\partial I_D}{\partial V_G}\right)_{V_D=const} = \frac{WC_i}{L}\mu_{FET}V_D. \quad (3)$$

The transconductance, which is a measure of the current carrying capability, is the ratio of the change in drain current and the change in gate voltage over a defined, arbitrarily small interval in the drain current vs. gate voltage curve. By plotting I_D versus V_G at a constant low V_D, the value of g_m is obtained from the slope of this plot as shown in Fig. 11b. High transconductance implies that transistor can run faster, and for good device performance, the channel geometry of the device is important. As shown in Eq. (3), the high ratio of channel width to channel length gives high transconductance.

For V_D more negative than V_G, I_D tends to saturate (saturation regime) owing to the pinch-off of the accumulation layer. In this regime, the variation of saturation drain current ($I_{D,sat}$) with gate voltage (V_G) can yield a field effect mobility (μ_{FET}) given by the relation [Katz, 1997; Haddon et al., 1995; Sirringhaus et al., 1997; Dimitrakopoulos et al., 1997; Garnier et al., 1998; Xu et al., 2000; Hu et al., 1999]:

$$I_{D,sat} = \frac{WC_i}{2L}\mu_{FET}(V_G - V_T)^2. \quad (4)$$

In the saturation regime, μ_{FET} can be calculated from the slope of $|I_D|^{1/2}$ vs. V_G. Differences can often be observed in mobility values calculated in the linear region and the saturation region. The linear region mobility can be affected by contact problems and in such cases there are departures from the linearity of the I_D vs. V_D curves which can lead to underestimation of mobility. In the saturation regime, when channel lengths are comparable to the gate insulator thickness or only a few times greater than that thickness, the I_D vs. V_D curves do not saturate and exhibit an upward trend at high V_D. Calculating the mobility in the saturation region from such devices can lead to erroneously high values [Dimitrakopoulos and Mascaro, 2001]. The extrapolation of the slope of the plot between $|I_D|^{1/2}$ and V_G to the V_G axis gives the threshold voltage (V_T). Most of the organic field effect thin film transistors (OFETs) have a negative V_T value indicating that OFETs are normally off type transistors [Kuo et al., 1998; Hu et al., 1999].

2. Current Modulation (I_{on}/I_{off}, on/off Current Ratio)

Current modulation is the ratio of the current in the accumulation mode over the current in the depletion mode. It is an important parameter for transistor applications and it depends on the mobility, charge density, conductivity and thickness of the semiconductor layer. The 'I_{off}' is defined as the case of little or no current flowing between the source and drain electrodes at a given source-drain voltage, while the 'I_{on}' refers to the substantial source-drain current

flows for the given source-drain voltage [Katz, 1997]. For many memory and display applications, a high on/off ratio exceeding 10^8 is a more important requirement than a high mobility [Sirringhaus et al., 1997]. An on/off ratio that is greater than 10^6 can be achieved by using organic semiconductors, which is high enough for transistor applications. On/off ratio is calculated from Eqs. (4) and (5) as [Dimitrakopoulos and Mascaro, 2001; Schön et al., 2000]

$$I_{off} = \frac{W}{L}\sigma d V_D \tag{5}$$

$$\frac{I_{on}}{I_{off}} = \frac{C_i \mu_{FET}(V_G - V_T)^2}{\sigma d V_D} \tag{6}$$

where μ_{FET} is the field effect mobility, σ is the conductivity, d is the thickness of the semiconductor, C_i is the capacitance per area of the gate insulator and V_D is the drain-source voltage. TFTs in practical applications attain the I_{off} regime under low bias, close to 0 V. OTFTs should be constructed with very low dopant concentration (low conductivity) and with a semiconducting layer as thin as possible as shown in Eq. (6).

3. Sub-Threshold Swing (S)

As shown in Fig. 11c, TFT does not turn off abruptly at the threshold voltage V_T as the on current equation would suggest. Instead, there is a sub-threshold region where the drain current varies approximately exponentially with gate voltage. For single crystal silicon FETs, the sub-threshold region is well-behaved and ideally the sub-threshold slope comes from the exponential activation of current with voltage compared to the thermal voltage. At room temperature, this gives a sub-threshold slope for drain current of about 60 mV/decade. Due to tail and midgap states, a-Si : H TFTs have a much larger sub-threshold slope, typically 0.3 to 1.5 V/decade. The sub-threshold slope for the pentacene TFTs is about 4-5 V/decade [Lin et al., 1997a] on the SiO_2 gate dielectric. Sub-threshold swings (S) less than 150 mV/decade can be possible in thin film transistors by improving the interface between active layer and the gate insulator [Schön et al., 2000b; Schön, 2001].

ELECTRICAL CHARACTERIZATION

1. Electrical Characterization of Semiconducting Layer

In Eqs. (3) and (6), the transconductance (or mobility) and I_{on}/I_{off} is dependent on μ_{FET} and μ_{FET}/σ. The mobility and conductivity of the semiconductor layer are important for transistor characteristics, and a good operation of the device requires a large mobility and low conductivity [Sirringhaus et al., 1997]. The (drift) mobility of the carriers (μ) is defined as the ratio of carrier drift velocity v_d and electric field E,

$$v_d = \mu E. \tag{7}$$

If we had any way of directly measuring the velocity of carriers, assuming we knew the electric field, we could directly find the mobility. In reality, the measurement of the velocity is difficult and we have to resort to more indirect methods.

Mobility can be determined by the following experimental methods either in a straightforward manner or more indirectly [Karl, 2002; Okubo, 2001; Schön, 2001; Schon, 2001; Schon and Batlogg, 2001; Brutting et al., 1995; Horowitz et al., 1998, 1999; Karl et al., 2000; Burland, 1974; Jarrett and Friend, 1995]. There are several most common methods to measure the mobility: Field Effect Transistor (FET) measurement, Hall measurement, Time of Flight (ToF) and Space Charge Limited Current (SCLC) method. For organic semiconductors, the most common technique is via FETs. In the FET method, the mobility can be extracted from the magnitude of the initial increase (with increasing gate voltage) of the current, caused by the driving field generated by a fixed voltage $V_D \ll V_G$ applied between the drain and source electrode. Mobility can also be obtained from the gate field dependence of the saturation current, obtained at high drain voltage $V_D > V_G$. The rather low mobility of the carriers in organic materials makes measuring in a Hall set up difficult. It can deviate from the mobility measured in other experiments. For instance, the assumption is made that all holes move with the same velocity. In fact, this is not true and the Boltzmann distribution is a much better approximation. The ToF method is probably the most direct way of measuring the velocity and hence the mobility of the carriers. Free carriers are generated by short pulses from an electron beam. Analysis of the current-time dependence observed in a short time after excitation gives the possibility of determining the effective carrier drift mobility and other parameters describing the charge transport. The DC current of a device can be divided into the following types. In the ohmic regime, the current is proportional to the electric field,

$$I \sim \mu V \tag{8}$$

where I, μ, V is current, carrier mobility and applied voltage respectively. The Space Charge Limited Current (SCLC) regime occurs when the equilibrium charge concentration (before charge injection) is negligible compared to the injected charge concentration. This will form a space charge cloud near the injecting electrode and the concentration of the space charge rapidly dies out away from the electrode. In this regime, the current is proportional to the square of the electric field. With the bias, the trap levels are filled. Above the trap-free voltage limit, the traps are filled and the device enters the trap-free SCLC [Schön et al., 1998; Sze, 1981] where

$$I \sim \mu V^2. \tag{9}$$

Since the results of the various measurements can be varying tremendously, we have to specify which method was used to measure the mobility. For example, although the largest field-effect mobility reported for sexithienyl based TFTs are near 0.1 cm^2/Vs, much larger mobility has been observed in bulk organic materials. In the anthracene case, several reported values of Hall mobilities for photogenerated carriers are about 1 to 10 cm^2/Vs range. The problem is that, thus far, these mobilities have not been useful for building electronic devices (though they have certainly been useful in transport physics studies and may be useful in applications such as organic metal replacements) [Lin et al., 1997a].

Eq. (6) shows that a very low conductivity value is required for good operation of organic devices [Garnier, 1998]. Various experimental techniques have been used for the calculation of conductivity. Among them, the methods commonly employed are the linear four probe and square probe array methods [Schroder, 1990; Wieder, 1979]. The most widely used method for measuring conductivity in the 10^1 to 10^6 S/cm range is the linear four-point probe technique. When characterizing thin layers, it is useful to introduce the

concept of resistance per unit area, or sheet resistivity. The sheet resistivity of a homogeneous layer is simply

$$\rho_s = \frac{\rho}{d} \tag{10}$$

where d is the thickness of the layer. Four probe tips are arranged in a linear array. Probe force, probe travel, tip radius and probe material must be selected with consideration of the resistivity, hardness, and thickness of the layer to be measured. It is customary to have the outer two probes carry current and the inner probes measure the resultant voltage. If the probe spacing is equal, then

$$\rho_s = \left(\frac{\pi}{\ln 2}\right) R_a = 4.532 R_a \tag{11}$$

where $R_a = V_a/I$ and represents the average of the two resistance values obtained by reversing the polarity of the current supply. This procedure eliminates any voltage offsets in the circuit.

2. Electrical Characterization of Dielectric Layer

The dielectric properties of the gate insulator are important in the performance of the OTFT device. Dielectric properties include breakdown field strength, dielectric constant and loss factor. For inorganic materials, these properties are relatively stable in terms of the frequency of the applied field and temperature but organic materials are not. For example, dielectric constant, or relative permittivity of the SiO_2 is 3.78 in the frequency of 10^2-10^{10} Hz and dielectric strength is as high as 10 MV/cm. But the dielectric constant of organic materials depends on the frequency and temperature, and the trend is quite complicated as shown in Fig. 12 [Osswald and Menges, 1996]. The dipole polarization of organic materials is complicated because of their interaction between backbone and functional groups. Higher value of C_i gives higher current flow in the device as shown in Eq. (3). As shown in the following equation, the higher the relative permittivity of the gate insulator material, the higher the value of C_i:

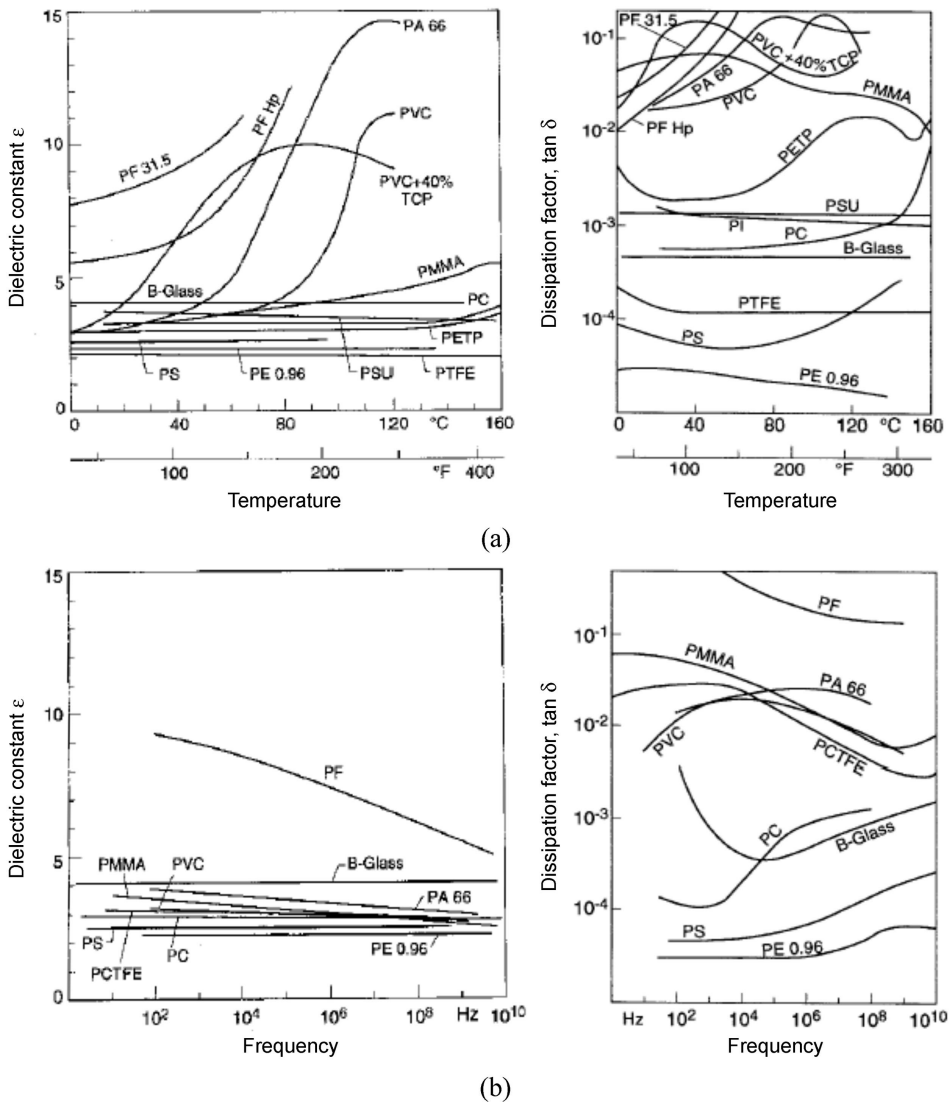


Fig. 12. Dielectric properties of various polymers in the various temperature and frequency. (a) Dielectric constant and dissipation factor of various polymers in the various temperature. (b) Dielectric constant and dissipation factor of various polymers in the various frequency.

$$C_i = \frac{\varepsilon_0 \varepsilon'}{d} \tag{12}$$

where C_i, ε_0, ε', d are the capacitance per unit area of the gate insulator, the permittivity of free space, relative permittivity (dielectric constant) and the thickness of the insulator layer respectively. The relative permittivity equations are as follows including the frequency response of the material,

$$\varepsilon_r = \frac{\varepsilon_s - \varepsilon_\infty}{1 - i\omega\tau} + \varepsilon_\infty \tag{13}$$

where ε_s, ε_∞, ω are static permittivity, unrelaxed permittivity and frequency respectively. τ is the relaxation time of the material which shows how fast the material responds to the applied field. Relative permittivity, ε_r, is a complex number defined as $\varepsilon_r = \varepsilon_0(\varepsilon' - i\varepsilon'')$. By separating ε_r into its real part and imaginary part, each part is obtained as

$$\varepsilon' = \frac{\varepsilon_s - \varepsilon_\infty}{1 + \omega^2\tau^2} + \varepsilon_\infty, \varepsilon'' = \frac{\varepsilon_s - \varepsilon_\infty}{1 + \omega^2\tau^2}\omega\tau. \tag{14}$$

Though ε' is only the real part of the relative permittivity, it is usually called relative permittivity or dielectric constant. ε' is a measure of the energy stored in the oscillations of the dipolar units. ε'' is called the dielectric loss or dissipation factor, because it is related to the energy dissipation in the material due to the internal friction. The energy loss per cycle heats the device under the following relationship

$$W \sim E^2\omega\varepsilon'' = E^2\omega\varepsilon'\tan\delta \tag{15}$$

where W is power, E is electric field, ω is frequency, ε' is relative permittivity, ε'' is dielectric loss and $\tan\delta$ is dielectric loss factor. This is the heat caused by internal friction of the molecular movements in the dielectric.

An applied alternating electric field interacts with the electric dipole moment of the device under test. As the frequency becomes larger, the slower mechanisms drop off and leave only the faster mechanisms to contribute to the dielectric storage (ε'). The dielectric loss factor (ε'') will correspondingly peak at each critical frequency. Dielectric relaxation is the result of a movement of dipoles or electronic charges due to a changing electric field in the frequency range of 10^2-10^{10} Hz. This mechanism is relatively slow when compared with ionic polarizations (about 10^{13} Hz, infrared region) or electronic polarizations (over 10^{15} Hz, ultra violet region). Frequency dependence of the polarization mechanisms in dielectrics is shown in Fig. 13 [Osswald and Menges, 1996] where χ is dielectric susceptibility, $\chi = \varepsilon_r - 1$. Only when sufficient time is allowed after the application of an electric field for the orientation to attain equilibrium with the maximum polarization, corresponding to the highest observable dielectric constant, be realized in a material. If time is allowed, then the observed dielectric constant is the static permittivity or static dielectric constant, ε_s. For SiO_2 in the frequency of 10^2-10^{10} Hz, maximum polarization is realized. If the polarization is measured immediately after the field is applied, not allowing time for dipole orientation, then the instantaneous dielectric constant, ε_∞, is observed. As can be seen in Fig. 12, dielectric properties change as a function of frequency and temperature for organic materials. The relaxation time, τ, occurs somewhere in between these extremes and this is energy absorption process. The loss peak occurs where $\omega_{max}\tau = 1$ and ω_{max} is the frequency of maximum loss peak. At room temperature, the relaxation times of the orientational polarization in crystals are 10^{-11} to 10^{-9} s. In amorphous solids and polymers, however, they can reach a few seconds or even hours, days and years, depending on the temperature. Relaxation time decreases with increasing temperature and decreasing size of polar group. The relationship between temperature and relaxation time is

$$\tau = \tau_0 \exp\left(\frac{E_a}{kT}\right). \tag{16}$$

where τ, T, E_a, k are relaxation time, temperature, activation energy and Boltzmann constant, respectively. τ_0 does not depend on the temperature [Scaife, 1989]. By combining Eqs. (14) and (16), it is possible to describe the temperature variation in the location of the loss peak ($\tan\delta_{max}$ and ε''_{max}) and loss peak moves higher frequency with increasing temperature [Scaife, 1989]. In the polymer, the scale of poling chain is changed with increasing temperature and also the relaxation accompanies the glass transition which occurs by the onset of segmental movements of the polymer chains. This is observed at the highest temperature for a given frequency or at the lowest frequency for a given temperature. At higher frequencies or lower temperature a relaxation is present which involves local intra-molecular movements. As can be seen in Fig. 12, the temperature dependence of the organic materials is quite complicated.

Dielectric strength is the maximum electric field that a dielectric can sustain before dielectric breakdown. Dielectric strength limits how much energy can be stored in a capacitor of fixed dimensions. Table 6 shows dielectric strength of various polymers at room temperature [Osswald and Menges, 1996]. To sustain the sweeping of voltage in the device operation, polymer dielectric layer should be thicker than inorganic dielectric layer because dielectric strength of organic material is smaller than inorganic material.

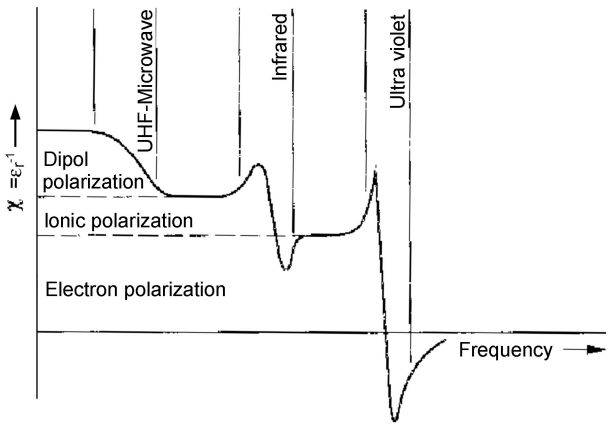


Fig. 13. Frequency dependence of the polarization mechanisms in dielectrics.

CONCLUSION

Intense research efforts so far have resulted in organic thin film transistors (OTFTs) with active layers such as α-6T, DH6T and penta-

Table 6. Dielectric strength of various polymers at room temperature

Polymer	Dielectric strength (MV/m)
ABS	25
Acetal (homopolymer)	20
Acetal (copolymer) acrylic	20
Acrylic	11
Cellulose acetate	11
CAB	10
Epoxy	16
Modified PPO	22
Nylon 66	8
Nylon 66+30% GF	15
PEEK	19
PET	17
PET+36% GF	50
Phenolic (mineral filled)	12
Polycarbonate	23
Polypropylene	28
Polystyrene	20
LDPE	27
HDPE	22
PTFE	45
UPVC	14
PPVC	30
SAN	25

cene deposited by high vacuum system. They showed high mobility and on/off ratio which were reasonably good enough for actual device utilization. To make OTFTs cost effective, it is required to deposit organic materials by simple solution processing technique. Most of the conjugated aromatics like pentacene are not soluble in common organic solvents and so precursor routes for those conjugated materials are used to prepare films. In this case, the long and high temperature conversion process is the major problem in terms of processing and compatibility with the metallic components of the device. It is desirable to synthesize polymeric or oligomeric materials that can be deposited at lower temperature.

It is imperative to improve the performance of OTFTs so that they can find applications in display drivers and pagers, and memory elements in transaction cards and identification tags. The performance of the OTFTS can be improved by proper selection of

1. active semiconducting material (polymers or small molecules with high carrier mobility),
2. gate dielectric material (polymers with high resistivity, high dielectric constant, and low loss value),
3. metal electrodes (metals which can give good ohmic contact),
4. device structure, dimension and spacing of the source and drain electrodes,
5. thickness of the active semiconductor layer and gate dielectric layer,
6. interface between active semiconductor and dielectric insulator.

Also a cost-effective processing technique and equipment should be developed for the deposition of each layer. Morphology of materials as a function of process parameters should be studied. Higher mobility can be achieved by reducing the number of grain boundaries and the number of crystal grains per unit area.

It is expected that in the near future, organic thin film transistors will find applications in mass produced information technology devices.

NOMENCLATURE

C_G : total capacitance on the gate [F]
C_i : capacitance per unit area of the gate insulator [F/cm^2]
d : thin film thickness [nm]
E : electric field [V/cm]
E_a : activation energy [J]
f_{max} : maximum frequency of operation [s^{-1}]
g_m : transconductance [S]
I : current [A]
I_D : drain current [A]
$I_{D,sat}$: saturated drain current [A]
I_{on}/I_{off} : on/off current ratio, dimensionless
k : Boltzmann constant [J/K]
L : gate channel length [nm]
R_a : average of the two resistance values [Ωcm]
R_S : sheet resistance [Ω/sq]
V : voltage [V]
V_a : measured voltage using four point probe [V]
V_D : drain voltage [V]
v_d : carrier drift velocity [cm/s]
V_G : gate voltage [V]
V_T : threshold voltage [V]
W : gate channel width [nm]
$\Delta\varepsilon$: relaxation strength, dimensionless
ε' : real part of the relative permittivity, relative permittivity, dimensionless
ε'' : imaginary part of the relative permittivity, dielectric loss, dimensionless
ε''_{max} : the peak of dielectric loss, dimensionless
ε_0 : the permittivity of free space [F/cm]
ε_r : relative permittivity, dimensionless
ε_s : static permittivity, static dielectric constant, dimensionless
ε_∞ : unrelaxed permittivity, instantaneous dielectric constant, dimensionless
μ : carrier mobility [cm^2/Vs]
μ_{FET} : field effect mobility [cm^2/Vs]
ρ : resistivity [Ωcm]
ρ_s : sheet resistivity of the homogeneous layer [Ω/sq]
σ : conductivity [S/cm]
τ : relaxation time [s]
τ_0 : relaxation time which does not depend on temperature [s]
ω : angular frequency [s^{-1}]
ω_{max} : frequency of maximum loss peak [s^{-1}]
$\tan\delta$: dielectric loss factor, dimensionless
$\tan\delta_{max}$: loss peak, dimensionless

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